

EG2104S Datasheet

MOS driver chip with
SD function

Version Change record

Version No	Date	Description
V1.0	October 10, 2017.	First draft of the EG2104S Datasheet

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EG2104S Datasheet V1.0

1. Features

- High-end suspension bootstrap power supply design, withstand voltage up to 600V
- Adapts to 5V, 3.3 V input voltages
- Maximum frequency support 500KHZ
- VCC and VB side supplies with undervoltage protection
- Low-side VCC voltage range 10V-20V
- Output current capability IO+/- 1.0 A/1.5 A
- Built-in dead zone control circuit
- SD input channel is active low, turning off the HO and LO outputs.
- Fewer peripheral devices
- Package form: SOP-8

2. Description

EG2104S is a cost-effective MOS transistor with SD function, IGBT transistor Gate Drive dedicated chip, integrated logic signal input processing circuit, dead zone control circuit, level displacement circuit, pulse filter circuit and output drive circuit, dedicated to brushless motor controller, power supply DC-DC drive circuit.

The high-end operating voltage of the EG2104S can reach 600V, and the low-end Vcc has a wide supply voltage range of 10V~20V. The chip input channel has a built-in 200k pull-down resistor, SD has a built-in 200k pull-down resistor, when the input is floating so that the upper and lower power MOS transistor is turned off, the output current capability IO+/- 1.0/1.5 A, using SOP8 package.

■ Application areas

- Mobile power supply high voltage fast charge switching power supply
- Wireless charging drive variable frequency pump controller
- DC-DC power supply
- Brushless motor driver
- High voltage Class-D power amplifier

3. Pin

3.1 Pin definition

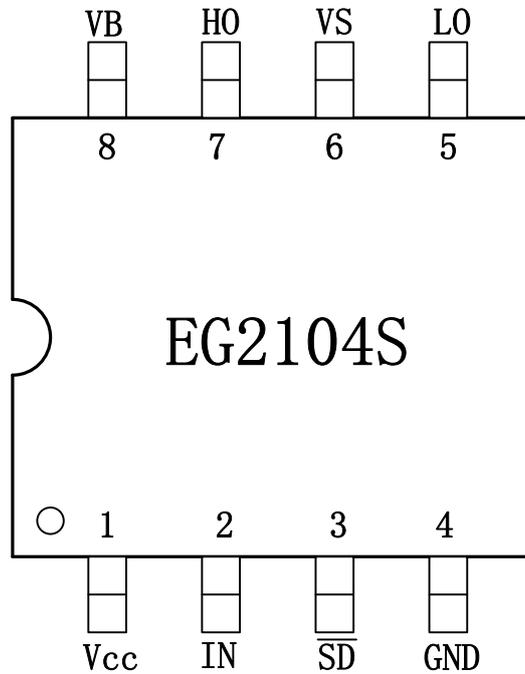


Figure 4-1. EG2104S pin definition

3.2 Pin description

Pin serial No	Pin name	I/O	Description
1	Vcc	Power	Chip power input, voltage range 9V-20V,an external high-frequency 0.1 uF bypass capacitor can reduce the high-frequency noise at the input of the chip
2	IN	I	Logic input control signal to control the output MOS transistor is turned on and off "0" corresponds to LO High,HO low. "1" corresponds to HO high,LO low.
3	\overline{SD}	I	Logic input control signal is active low, forcing the LO,HO output low. "1 " allows LO and HO to be controlled with the IN input. "0" forces the LO and HO outputs low.
4	GND	GND	The ground end of the chip.
5	LO	O	The output controls the conduction and shutdown of the low-side MOS transistor
6	VS	O	High-end suspended Ground end
7	HO	O	The output controls the on and off of the high-side MOS transistor
8	VB	Power	High-end suspended power supply

4. Block diagram

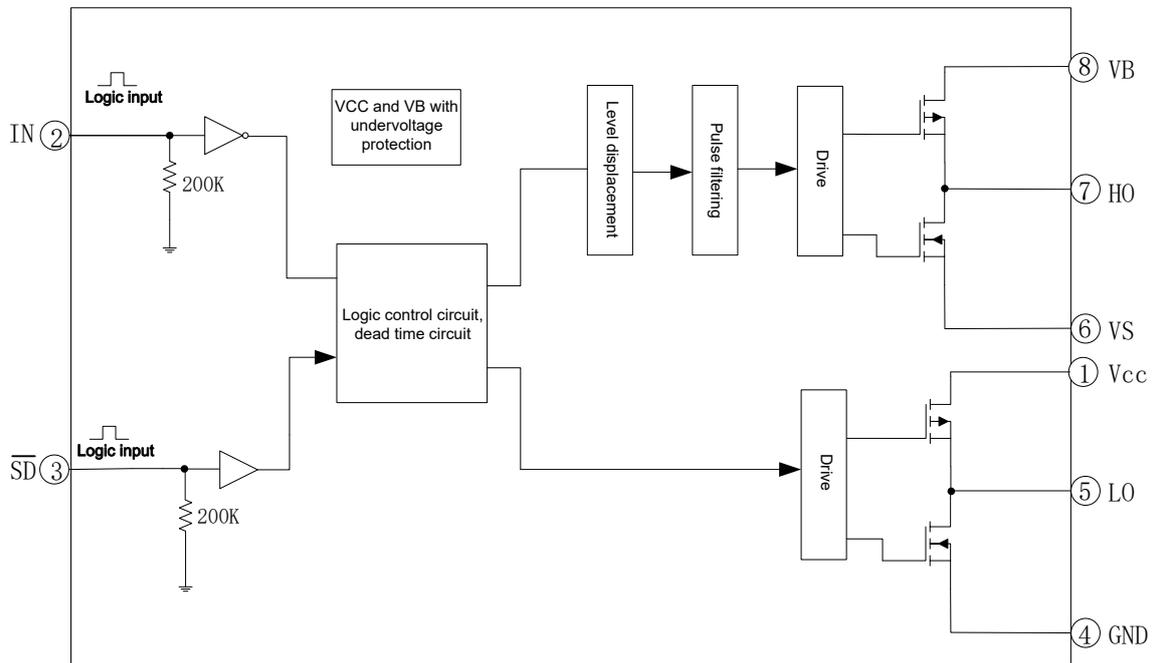


Figure 5-1. EG2104S internal circuit diagram

5. Typical application circuit

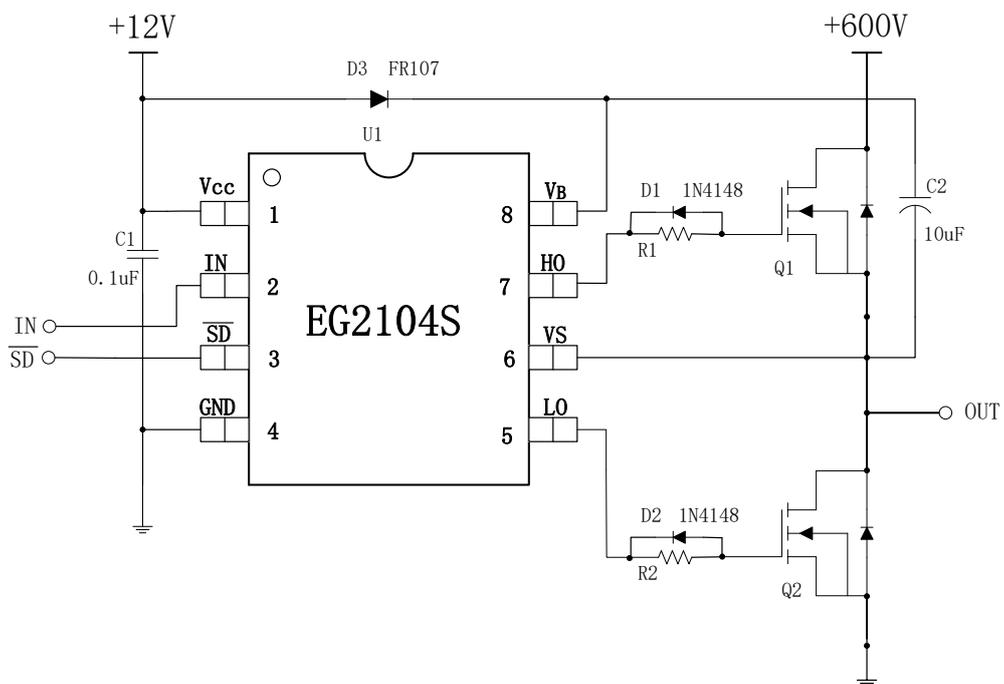


Figure 6-1. EG2104S typical application circuit diagram

6. Electrical characteristics

6.1 Limit parameters

Without further explanation, at TA=25°C conditions

Symbols	Parameter name	Test conditions	Min.	Max.	Units
High side floating absolute voltage	VB	-	-0.3	600	V
High side floating supply offset voltage	VS	-	VB-20	VB+0.3	V
High side floating supply offset voltage	HO	-	VS-0.3	VB+0.3	V
Low side output voltage	LO	-	-0.3	VCC+0.3	V
Low side and logic fixed supply voltage	VCC	-	-0.3	20	V
Logic input voltage (HIN & LIN)	IN	-	-0.3	VCC+0.3	V
Low channel logic signal input level	\overline{SD}	-	-0.3	6	V
TA	Ambient temperature	-	-45	125	°C
Tstr	Storage temperature	-	-55	150	°C
TL	Soldering temperature	T=10S	-	300	°C

Note: exceeding the listed limit parameters may cause permanent damage to the chip, operating in extreme conditions for a long time will affect the reliability of the chip.

6.2 Typical parameters

Without further explanation, at TA=25°C, Vcc=15v, load capacitance CL=1NF conditions

Parameter name	Symbols	Test conditions	Min.	Typical	Max.	Units
Power supply	Vcc	-	10	15	20	V
Quiescent current	Icc	Input dangling, Vcc=15V	-	100	200	uA
Input logic signal high potential	Vin(H)	All input control signals	2.5	-	-	V
Input logic signal low potential	Vin(L)	All input control signals	-0.3	0	1.0	V
Current at the high level of the input logic signal	Iin(H)	Vin=5V	-	-	30	uA
Input logic signal low current	Iin(L)	Vin=0V	-10	-	-	uA
VCC supply undervoltage shutdown feature						
VCC turn-on voltage	Vcc(on)	-	7.6	8.6	9.6	V
VCC shutdown voltage	Vcc (off)	-	7.1	8.1	9.1	V
VB supply undervoltage shutdown feature						
VB turn-on voltage	VB(on)	-	6.8	7.8	8.8	V
VB shutdown voltage	VB (off)	-	6.6	7.6	8.6	V
Low-side output LO switching time characteristics						
On delay	Ton	See Figure 7-1	-	800	940	ns
Off delay	Toff	See Figure 7-1	-	160	240	ns
Rise Time	Tr	See Figure 7-1	-	150	250	ns
Descent time	Tf	See Figure 7-1	-	75	175	ns
High-side output HO switching time characteristics						
On delay	Ton	See Figure 7-2	-	800	940	ns
Off delay	Toff	See Figure 7-2	-	160	240	ns
Rise Time	Tr	See Figure 7-2	-	150	250	ns
Descent time	Tf	See Figure 7-2	-	75	175	ns
Dead time characteristics						
Dead time	DT	See Figure 7-3, No load capacitance CL=0	500	640	800	ns
IO output maximum drive capability						
IO output pull current	IO+	Vo=0V, VIN=VIH PW≤10uS	-	1.0	-	A

IO output sink current	IO-	$V_o=12V, V_{IN}=V_{IL}$ $PW \leq 10\mu S$	-	1.5	-	A
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6.3 Switching time characteristics and dead time waveform diagram

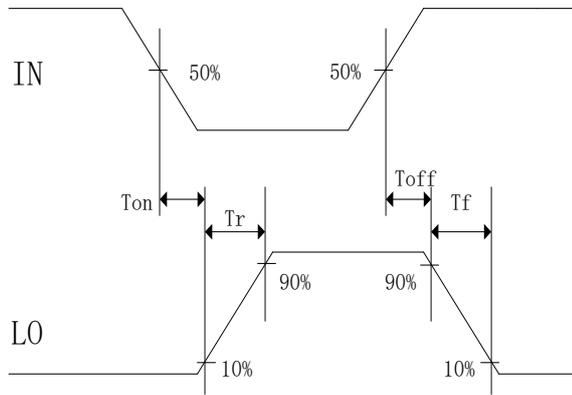


Figure 7-1. Low-side output LO switching time waveform diagram

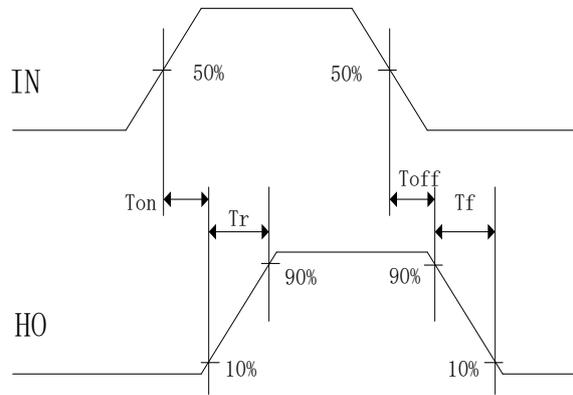


Figure 7-2. High-side output HO switching time waveform diagram

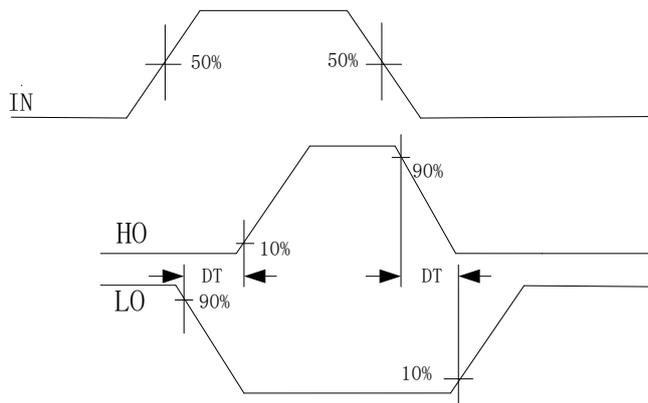


Figure 7-3. Dead time waveform diagram

7. Application design

7.1 VCC terminal supply voltage

For different MOS transistor, select a different drive voltage, chip supply voltage range of 10V-20V.

7.2 Input logic signal requirements and output driver characteristics

The main functions of the EG2104S are logic signal input processing, dead time control, level translation function, floating bootstrap power structure and upper and Lower Bridge totem pole output. Logic signal input high threshold of 2.5 V or more, low threshold of 1.0 V or less, the requirements of the output current of the logic signal is small, you can make the MCU output logic signal is directly connected to the EG2104S input channel.

Up to 1.0 A and the maximum output current up to 0.6 A, the high-end arm channel can withstand 600V voltage, the input logic signal and the output control signal conduction delay between small, low-end output opening conduction delay of 800ns, turn-off conduction delay of 160ns, high-end output opening conduction delay of 800ns, turn-off conduction delay of 160ns. The rise time of the low-side output is 150ns, the fall time of the shutdown is 75ns, the rise time of the high-side output is 150ns, the fall time of the shutdown is 75ns.

Input signal and output signal logic function diagram shown in Figure 8-2 :

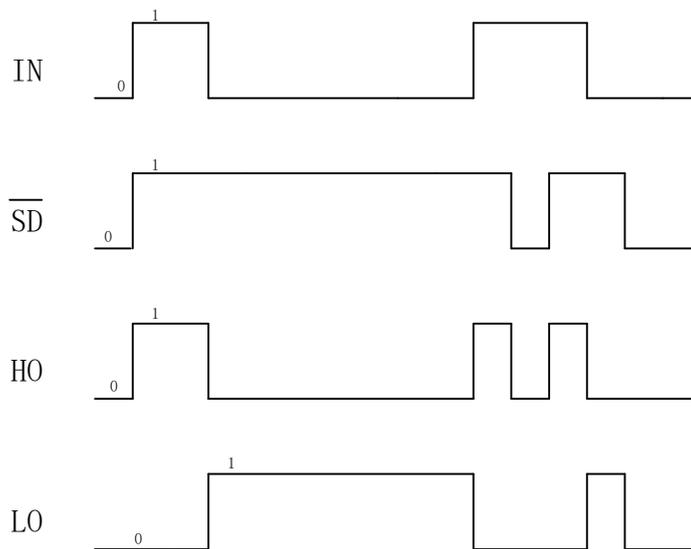


Figure 8-2. Input signal and output signal logic function diagram

Logic truth table for input and output signals:

Input		Output	
Input and output logic			
IN (pin 2)	SD (pin 3)	HO (Pin 7)	LO (pin 5)
0	0	0	0
1	0	0	0
0	1	0	1
1	1	1	0

From the truth table, the input logic signal SD is "0", regardless of IN is "1" or "0", The Drive control output HO, LO while "0", the upper and lower power tube is turned off simultaneously; when the input logic signal SD is "1", IN is "0", HO output is "0", LO output is "1"; when the input logic signal SD is "1", IN is "1", HO output is "1", LO output is "0".

7.3 Bootstrap circuit

EG2104S using Bootstrap suspension drive power supply structure greatly simplifies the drive power supply design, only one way to complete the power supply voltage VCC high-end N-channel MOS transistor and low-end N-channel MOS transistor driving two power switching devices, to the practical application of great convenience. EG2104S can use an external bootstrap diode as shown in Figure 8-3 and a bootstrap capacitor to automatically complete the bootstrap boost function, assuming that the lower tube is turned on, the upper tube is turned off during the VC bootstrap capacitor has been charged to a sufficient voltage ($V_c = V_{CC}$), when the HO output is high on the tube is turned on, the lower tube is turned off, the voltage on the VC bootstrap Capacitor will be equivalent to a voltage source as an internal driver VB and VS, complete the high-end N-channel MOS transistor.

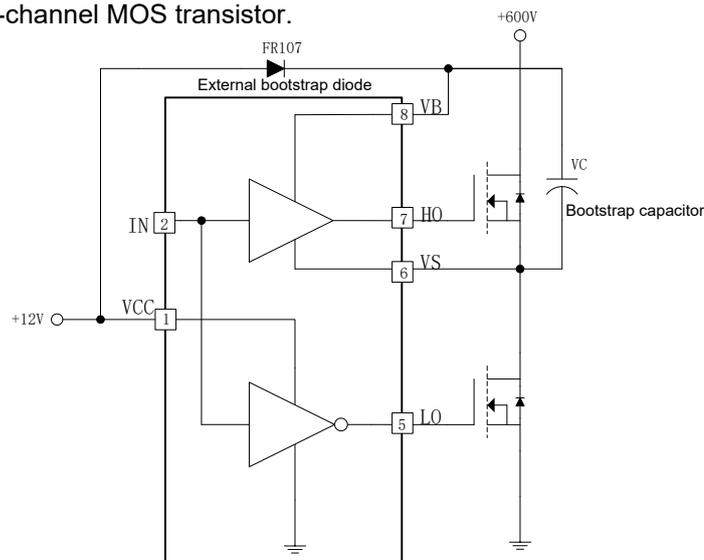


Figure 8-3. EG2104S bootstrap circuit structure

8. Package size

8.1 SOP8 Package size

